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Modeling of Signals in Subnanosecond Analog-to-Digital Information Converters

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Abstract. The mathematical model and methods of calculation of the layout structure of comparator signal circuits with distributed parameters are presented. The algorithm of computer formulation and solving of equations of transfer functions of comparator circuits is provided. Theoretical substantiation of optimizing the micro-layout of large-scale integration circuits of parallel subnanosecond analog-to-digital converters (ADC) is proposed.

The signal modeling and investigation of transitional processes in comparator circuits of the subnanosecond range 6-, 8-bit ADC of different layouts are presented. It has been determined that the transitional process quality in inputs of comparator blocks strongly depends on the signal circuit layout architecture, the compatibility of wave resistances of signal microstrip lines and on the number of branches to comparator bloks.The designed layouts of the 6-bit subnanosecond range ADC comparator circuit with different layout structures are presented. Modeling of equivalent circuits of the designed layouts was performed and the modeling results are presented.The architecture of topology for comparators circuits presented here allows the developing of gigahertz 6- and 8-bit analog-to-digital information converter.

Key words: analog-digital conversion, data conversion, parallel architecture, modeling.

1. Introduction

With the data flow increase, fast analog-to-digital systems of information processing are widely developed. The data processing rate in modern digital systems is about 20–30 Gb/s. Therefore for the telemetric, radiolocational and optoelectronic communication systems, which operate on a real time scale, precise wide-band analog-to-digital converters are needed to convert analog information into digital. The speed of modern ADC ranges only up to 4–8 Gb/s. In literature, problems of designing microwave band analog circuits are recently receiving much attention (Aguileva *et. al.*, 1999; Celik *et. al.*, 1999; Davis *et. al.*, 2000; 2001; Ismail *et. al.*, 1999; 2002; Zheng *et. al.*, 2000; 2001). The reduction of the influence of interelemental signal line wave parameters on the converter operating speed is an important problem.

When designing very fast ADC, the wide-band signal delay and the form distortion due to reflections in electrically noncompatible circuits of distributed parameters should

be evaluated. The model of the microwave ADC comparator circuit and the signal calculation technique were developed and transitional processes in the 6- and 8-bit GHz ADC analog comparator circuit were investigated.

The generalized technique of the signal modeling in the comparator circuits of fast analog-to-digital converters (ADC) is presented in (Marcinkevičius, 1992). We will consider the application of this technique to the calculation of the signal form in the flash ADC comparator inputs when microstrip signal interconnection lines are with distributed parameters.

To decrease the sampling error, the converter layout architecture should be such that the difference $\Delta\tau_{ST}$ between the delay times of the analog signal and the clock pulses for all comparators is constant and does not exceed the allowable aperture time, i.e.,

$$\tau_{Si} - \tau_{Ti} = \Delta\tau_{ST} \leqslant \Delta t_a = \frac{1}{2\pi f_m \left(2^b - 1\right)}, \tag{1}$$

where τ_{Si} and τ_{Ti} are delay times of the analog signal and clock pulses in the signal and clock pulse lines for the ith comparator; f_m is the maximum frequency of the signal spectrum; b is the number of bits and Δt_a is the allowable aperture uncertainty time.

In this regard, the optimal structure of the ADC comparator circuit layout would be such in which for each ith comparator delay times of the signal and the clock pulses would be equal, i.e.,

$$\tau_{Si} = \tau_{Ti} = R_{eq.S}C_{eq.S} = R_{eq.T}C_{eq.T}, \tag{2}$$

where $R_{eqS}, C_{eqS}, R_{eqT}$ and C_{eqT} are equivalent active resistances and capacities in the signal and time pulse transfer circuits, respectively.

The structure of 6-bit (64 comparators) ADC layout close to the optimal is shown in Fig. 1. Here the lengths of the signal and clock microstrip lines from respective voltage sources E_S and E_T to each ith comparator are equal. The analog signal along with the clock pulses for the comparator blocks K_I, K_{II}, K_{III} and K_{IV} are transmitted in parallel while to comparators inside of each $K_1 - K_{16},\ K_{17} - K_{32},\ K_{33} - K_{48}$ and $K_{49} - K_{64}$ block are propagated due to serial transmission. The divider array resistors $R_1, R_2 \ldots, R_{65}$ of reference voltages U_{REF1} and U_{REF2} are arranged so that the influence of the comparator input currents is minimum.

Let us discuss the technique of the signal calculation in the input and output circuits of comparators when input and output impedances of comparators $K_1, K_2 \ldots, K_{64}$ are equal and the signal microstrip lines are with least losses and identical longitudinal parameters.

2. Composition for the Signal Calculation Equation

Signal Calculation Equations

For the calculation of the signal form in the comparator inputs, we assume that the impedance parameters of all comparators are equal and the signal line losses are small.

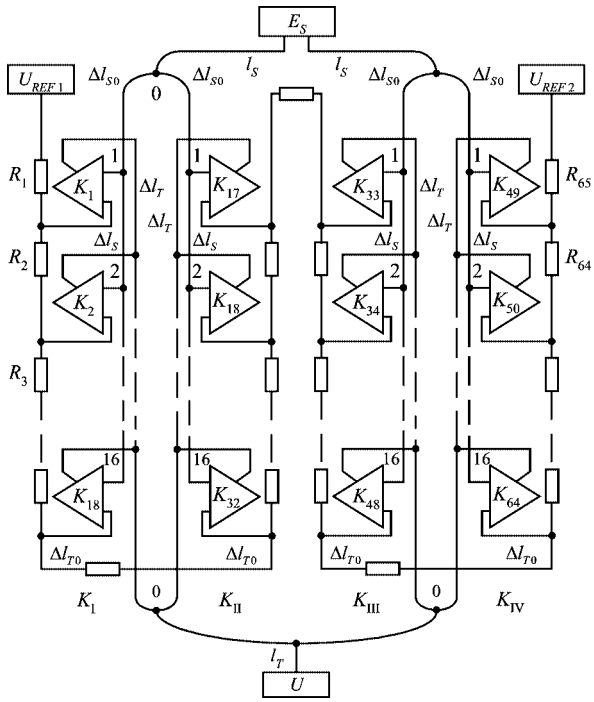

Fig. 1. Diagram of the 6-bit ADC comparator layout: U_{REF1} and U_{REF2} – the circuits of the divider array resistors $R_1, R_2, \ldots R_{65}$ of reference voltages; E_S – the voltage source of the analog signal; U_T – the voltage source of clock pulses; $K_I, K_{II}, K_{III}, K_{IV}$ – comparator blocks of 16 comparators; l_S, l_T – line lengths of the signal and clock pulses from the voltage source to the comparator attachment point "0"; Δl_S, Δl_T – the line section lengths between separate comparators in the block; Δl_{S0}, Δl_{T0} – line section lengths from point "0" to the first comparator in the block.

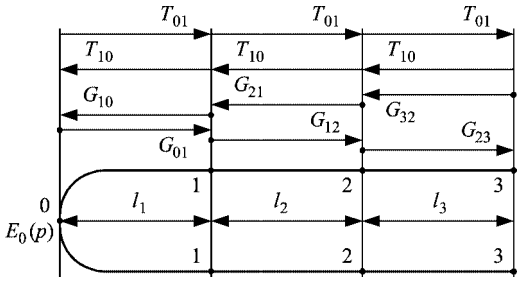

Fig. 2. A graphical diagram of the ADC comparator connection fragment.

We consider the signal forms in the dispersion-free frequency range. Then mathematical expressions of transmission functions of the circuit diagram become simpler.

For the calculation of signals in the inputs of comparators, a graphical diagram of the ADC basic fragment (Fig. 2) with the shown signal circuit functions T and G (with indices) for the propagating and reflected waves was developed.

The voltage equation in the input of the ith comparator is as follows (Marcinkevičius, 1988; Marcinkevičius, 1992):

$$U_i\,(p,\tau) = \sum_{j=i}^{z} U_{ij}\,(p,\tau_{ij}), \tag{3}$$

where $U_{ij}(p,\tau_{ij})$ is the jth wave voltage in the input of the ith comparator; $\tau_{ij} = \sum_{k=1}^{m_j} a_{jk}\tau_k$ is the delay time of the jth wave; τ_k is the delay time of the kth line section; a_{jk} is the coefficient showing how many times the wave has passed the kth line section; m_j is the number of line sections the jth wave has passed; z is the number of waves having passed to the ith load and p is the operator.

The jth wave voltage in the input of the ith comparator can be expressed by the operator equation (Marcinkevičius, 1992):

$$\begin{aligned} U_{ij}\Big(p,\tau_{ij}\Big) &= E_0\Big(p\Big)V_{ij} \\ &= E_0\Big(p\Big)\Big[\prod_{k=1}^{n} T_{(k-1)k}^{q_k}\Big]\Big[\prod_{k=1}^{n-1} T_{k(k-1)}^{S_k}\Big]\Big[\prod_{k=1}^{n} G_{(k-1)k}^{r_k}\Big]\Big[\prod_{k=1}^{n} G_{k(k-1)}^{g_k}\Big], \end{aligned} \tag{4}$$

where q_k, S_k, r_k, g_k are integer positive numbers, whose values depending on the time moment after the signal feed can be 0, 1, 2, $\ldots, M$; n is the load order number; $E_0(p)$ is the signal source voltage; T and G with indices are transfer functions of incident and reflected waves, expressed by the reflection coefficients k and signal transmission coefficients P at comparator connection points.

The equivalent circuit of the ADC signal transmission circuit, composed of the signal source D_0, the microstrip line with distributed parameters and the comparator D_1, is presented in Fig. 3.

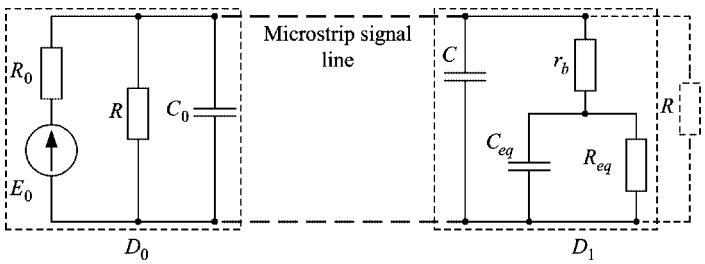

Fig. 3. Equivalent circuit of the signal source and the comparator input: D_0 – the analog signal source; D_1 – the comparator input impedance whose parameters C, C_{eq}, r_b, R_{eq} – the parasitic input capacitance, the equivalent input capacitance of the transistor, the base and equivalent input resistance, respectively.

The signal circuit transfer function V_{ij} for any ith comparator is expressed by an equation (Marcinkevičius, 2000):

$$V_{ij} = \beta_{eq}\left(\frac{P+p\left(\tau_2-\tau_1\right)}{1+p\tau_2}\right)^{q_j}\left(\frac{P_0^*}{1+p\tau_0}\right)^{s_j}\left(\frac{P_c+p\left(\tau_{2c}-\tau_{1c}\right)}{1+p\tau_{2c}}\right)^{r_j} \times\left(\frac{k^*-p\tau_1}{1+p\tau_2}\right)^{m_j}\left(\frac{k_0^*-p\tau_0}{1+p\tau_0}\right)^{n_j}\left(\frac{k_c^*-p\tau_{1c}}{1+p\tau_{2c}}\right)^{d_j}, \tag{5}$$

where $\tau_1 = C_{eq}R_{eq}, \tau_2 = r_bC$ and $\tau_3 = \left(r_b+R_{eq}\right)C$ are time constants; $\beta_{eq} = \exp\left(-\gamma l_{eq}\right)$ is the signal line equivalent transfer function; l_{eq} is the equivalent line length; *q, s, r* are coefficients showing how many times the wave passed the comparator attachment point up to the time moment under consideration; *m, n, d* are coefficients showing how many times the ith wave was reflected from the comparators up to the time moment under consideration; P and k with indices are transfer and reflection coefficients at comparator attachment points.

Voltages in the comparator inputs, i.e., at points "0", "1", "2", "3" (Fig. 2), when "m" reflected waves arrived from the line end, can be expressed in equation forms as

$$U_{\text{“0”}} = E_0\left[1+T_{01}\sum_{i=1}^{m}\left(T_{12}T_{23}G_{32}T_{21}T_{10}\right)^i G_{01}^{i-1}\right]+\Delta U_{\text{“0”}}, \tag{6}$$

$$U_{\text{“1”}} = E_0T_{01}\left[1+\sum_{i=1}^{m}\left(T_{12}T_{23}G_{32}T_{21}\right)^i\left(T_{10}G_{01}\right)^{i-1}\right]+\Delta U_{\text{“1”}}, \tag{7}$$

$$U_{\text{“2”}} = E_0T_{01}\left[T_{12}+\sum_{i=1}^{m}\left(T_{12}T_{23}G_{32}\right)^i\left(T_{21}T_{10}G_{01}\right)^{i-1}\right]+\Delta U_{\text{“2”}}, \tag{8}$$

$$U_{\text{“3”}} = ET_{01}\left[T_{12}T_{23}+\sum_{i=1}^{m}\left(T_{12}T_{23}\right)^i\left(T_{21}T_{12}G_{01}G_{32}\right)^{i-1}\right]+\Delta U_{\text{“3”}}. \tag{9}$$

Due to inner reflections, equations of voltages $\Delta U_{\text{“0”}}$, $\Delta U_{\text{“1”}}$, $\Delta U_{\text{“2”}}$, $\Delta U_{\text{“3”}}$ are derived as (6)–(9), only instead of the voltage E_0 the reflected wave equations are written:

$$E_{0\text{“1”}} = E_0T_{01}\left(T_{12}T_{23}G_{32}T_{21}T_{10}G_{01}\right)^{m-1}G_{10}, \tag{10}$$

$$E_{0\text{“2”}} = E_0T_{01}T_{12}^m\left(T_{23}G_{32}T_{21}T_{10}G_{01}\right)^{m-1}G_{21}T_{10}, \tag{11}$$

$$E_{0\text{“3”}} = E_0T_{01}\left(T_{12}T_{23}G_{32}T_{21}\right)^m\left(T_{10}G_{01}\right)^{m-1}G_{12}T_{23}G_{32}T_{21}T_{10}. \tag{12}$$

Reflections pass from the first comparator block K_I to the second K_{II} and vice versa. The voltage equations due to cross reflections in the comparator blocks are expressed in equation forms as

$$\Delta U_{\text{“0”}}\left(K_{\mathrm{I}} \Leftrightarrow K_{\mathrm{II}}\right) = E_0 T_{03}\left(G_{30}G_{03}\right)^{m-1} T_{01} \sum_{i=1}^{m_1} G_{10}^{i} G_{01}^{i-1}$$
$$+ E_0 T_{02}\left(G_{20}G_{02}\right)^{n-1} T_{01} \sum_{i=1}^{m_1} G_{10}^{i} G_{01}^{i-1}$$
$$+ E_0 T_{03}\left(G_{30}G_{03}\right)^{n-1} T_{02} \sum_{i=1}^{m_1} G_{20}^{i} G_{02}^{i-1}$$
$$+ E_0 T_{01}\left(G_{10}G_{01}\right)^{n-1} T_{02} \sum_{i=1}^{m_1} G_{20}^{i} G_{02}^{i-1}$$
$$+ E_0 T_{01}\left(G_{10}G_{01}\right)^{n-1} \times T_{03} \sum_{i=1}^{m_1} G_{30}^{i} G_{03}^{i-1}$$
$$+ E_0 T_{02}\left(G_{20}G_{02}\right)^{n-1} T_{03} \sum_{i=1}^{m_1} G_{30}^{i} G_{03}^{i-1}, \tag{13}$$

$$\Delta U_{\text{“1”}}\left(K_{\mathrm{I}} \Leftrightarrow K_{\mathrm{II}}2\right) = \left[E_0 T_{03}\left(G_{30}G_{03}\right)^{n-1} T_{01} G_{10}^{n} G_{01}^{n-1}\right]\left[T_{01}\sum_{i=1}^{m_2}\left(G_{10}G_{01}\right)^{i-1}\right]$$
$$+ \left[E_0 T_{02}\left(G_{20}G_{02}\right)^{n-1} T_{01} G_{10}^{n} G_{01}^{n-1}\right]\left[T_{01}\sum_{i=1}^{m_2}\left(G_{10}G_{01}\right)^{i-1}\right], \tag{14}$$

$$\Delta U_{\text{“2”}}\left(K1 \Leftrightarrow K2\right) = \left[E_0 T_{03}\left(G_{30}G_{03}\right)^{n-1} T_{02} G_{20}^{n} G_{02}^{n-1}\right]\left[T_{02}\sum_{i=1}^{m_3}\left(G_{20}G_{02}\right)^{i-1}\right]$$
$$+ \left[E_0 T_{01}\left(G_{10}G_{01}\right)^{n-1} T_{02} G_{20}^{n} G_{02}^{n-1}\right]\left[T_{02}\sum_{i=1}^{m_3}\left(G_{20}G_{02}\right)^{i-1}\right], \tag{15}$$

$$\Delta U_{\text{“3”}}\left(K_{\mathrm{I}} \Leftrightarrow K_{\mathrm{II}}\right) = \left[E_0 T_{01}\left(G_{10}G_{01}\right)^{n-1}\ T_{03} G_{30}^{n} G_{03}^{n-1}\right]\left[T_{03}\sum_{i=1}^{m_4}\left(G_{30}G_{03}\right)^{i-1}\right]$$
$$+ \left[E_0 T_{02}\left(G_{20}G_{02}\right)^{n-1} T_{03} G_{30}^{n} G_{03}^{n-1}\right]\left[T_{03}\sum_{i=1}^{m_4}\left(G_{30}G_{03}\right)^{i-1}\right], \tag{16}$$

where m_1, m_2, m_3, m_4 is the number of cross waves passing the point “0”.

The voltage in the input of each comparator, i.e., at points “1”, “2”, “3” of Fig. 2, for the preselected number “z” of waves is calculated according to (3).

The time function of the voltage in the ith comparator input is obtained from (1) using the Hewside theorem and is expressed by an equation (Marcinkevičius, 2000):

$$U_{ij}(t)=\Big[H_{11}+H_{21}\mathrm{e}^{-\left(\frac{t-\tau_{eq}}{\tau_f}\right)}+H_{31}\mathrm{e}^{-\left(\frac{t-\tau_{eq}}{\tau_{0\mathrm{eq}}}\right)}+H_{41}\,(t-\tau_{eq})^{m_4-1}\,\mathrm{e}^{-\left(\frac{t-\tau_{eq}}{\tau_2}\right)}$$
$$+\,H_{42}\,(t-\tau_{eq})^{m_4+2}\,\mathrm{e}^{-\left(\frac{t-\tau_{eq}}{\tau_2}\right)}+\ldots$$
$$+H_{NM_N}\mathrm{e}^{-\left(\frac{t-\tau_{eq}}{\tau_{2k}}\right)}\Big]\left(P^{*q_j}P_0^{*s_j}P_c^{*r_j}k^{*m_j}k_0^{*n_j}k_c^{*d_j}\right)A, \tag{17}$$

where H_{NM_N} are coefficients calculated by differentiating the transfer function M_N times and by finding roots of the obtained M equations; τ_k is the time constant of comparator input circuits.

Technique of Equation Composition for Calculation of Voltages in Comparator Inputs

By applying the wave motion model and the transfer functions T and G at comparator connection points, the signal calculation technique in ADC circuits of the signal transmission to comparators was developed. As an example, a parallel-series circuit is presented in Fig. 2. In the figure only comparator connection points are shown and transfer functions are indicated.

The equations of the calculation of transfer functions Q and K in voltage equations 6–16 for the composed signal circuit equivalent scheme (Fig. 3) are presented in Table 2.

Voltage expressions in the first line comparator inputs are presented in Table 1. Voltage expressions in the second and third line comparator inputs are derived in the same way. With any number of comparators, equations are derived in the same way.

The developed technique of automated composition of equations and calculation allows computer modeling of signal transitional processes in the flash ADC comparator inputs.

Table 1

Voltages in comparator inputs in the first line

"3"	"2"	"1"	"0"
$U_{21}T_{23}=U_{31}$	$U_{11}T_{12}=U_{21}$	$ET_{01}=U_{11}$	E
$\longrightarrow$	$U_{31}G_{32}=U_{22}$	$U_{22}T_{21}=U_{12}$	$U_{12}T_{10}=U_{01}$
$U_{23}T_{23}=U_{32}$	$U_{13}T_{12}=U_{23}$	$U_{01}G_{01}=U_{13}$	$\longleftarrow$
.....	.....	.....	.....
U_{3m}	U_{2k}	U_{1p}	U_{0n}
		$\boxed{U_{11}}\longrightarrow$	$U_{11}G_{10}=U_{0(n+1)}$
$U_{2(k+1)}T_{23}=U_{3(m+1)}$	$U_{1(p+1)}T_{12}=U_{2(k+1)}$	$U_{0(n+1)}G_{01}=U_{1(p+1)}$	$\longleftarrow$
$\longrightarrow$	$U_{3(m+1)}G_{32}=U_{2(k+2)}$	$U_{1(k+2)}T_{21}=U_{2(p+2)}$	$U_{1(p+2)}T_{10}=U_{2(n+2)}$
.....	.....	.....	.....
$U_3=\sum_{i=1}^{q_3}U_{3i}$	$U_2=\sum_{i=1}^{q_2}U_{2i}$	$U_1=\sum_{i=1}^{q_1}U_{1i}$	$U_0=\sum_{i=1}^{q_0}U_{0i}$

Table 2

Mathematical expressions of transfer functions

Arbitrary signs and symbols	Mathematical expression
$T=T_{01}=T_{12}=T_{21}$	$T=\beta_s\frac{(1+k^*)+p(\tau_2-\tau_1)}{1+p\tau_2}$
$T_0=T_{10};\ T_c=T_{23}$	$T_0=\beta_s\frac{1+k_0^*}{1+p\tau_0};\ T_c=\beta_s\frac{(1+k_c^*)+p(\tau_{2c}-\tau_{1c})}{1+p\tau_{2c}}$
β_s	$-\Delta l_s\left(p\sqrt{LC_1}+\frac{RC_1+LG}{2\sqrt{LC_1}}\right)$ $\beta_s=\mathrm{e}$
$G_0=G_{10};\ G_1=G_{01}$	$G_0=\frac{(1+k_0^*)(k-p\tau_1)}{(1+p\tau_0)[(1+k^*)+p(\tau_2-\tau_1)]};\ G_1=\frac{[(1+k^*)+p(\tau_2-\tau_1)](k_0^*+p\tau_0)}{(1+k_0^*)(1+p\tau_2)}$
$G_2=G_{32};\ G_3=G_{23}$	$G_2=\frac{[(1+k^*)+p(\tau_2-\tau_1)](k_c^*+p\tau_{1c})}{(1+p\tau_2)[(1+k_c^*)+p(\tau_{2c}-\tau_{1c})]};\ G_3=\frac{(k^*-p\tau_1)[(1+k_c)+p(\tau_{2c}-\tau_{1c})]}{(1+p\tau_{2c})[(1+k^*)+p(\tau_2-\tau_1)]}$
$k_0=k_{01};\ k_c=k_{32}$	$k_0=\frac{k_0^*-p\tau_0}{1+p\tau_0};\ k_c=\frac{k_c^*-p\tau_{1c}}{1+p\tau_{2c}}$
$k=k_{10}=k_{12}=k_{21}=k_{23}$	$k=\frac{k^*-p\tau_1}{1+p\tau_1}$
k_0^*	$k_0^*=\frac{R_e(2-N)-Z_0}{R_eN+Z_0}$; N – *number of comparator blocks connected in parallel*
$k^*;\ k_c^*$	$k^*=\frac{Z_0}{2(r_b+R_{ekv})+Z_0};\ k_c^*=\frac{R_{ekv.c}-Z_0}{R_{ekv.c}+Z_0}$,
$\tau_0;\ \tau_1$	$\tau_0=C_0\frac{R_eZ_0}{NR_e+Z_0};\ \tau_1=\lvert k^*\rvert\cdot[C_{ekv}R_{ekv}+C(r_b+R_{ekv})]$
$\tau_2;\ \tau_{1c}$	$\tau_2=C_{ekv}R_{ekv}\lvert k^*\rvert+C_{ekv}\frac{2r_bR_{ekv}}{2(r_b+R_{ekv})+Z_0};\ \tau_{1c}=C_{ekv}\frac{Z_0R_1-R_cR_2}{R_{ekv.c}+Z_0}+C\frac{Z_0R_{ekv.c}}{Z_0+R_{ekv.c}}$
τ_{2c}	$\tau_{2c}=C_{ekv}\frac{Z_0R_1+R_cR_2}{R_{ekv.c}+Z_0}+C\frac{Z_0R_{ekv.c}}{Z_0+R_{ekv.c}}$
$R_1;\ R_2;\ R_{ekv.c}$	$R_1=\frac{R_{ekv}(r_b+R_c)}{R_{ekv}+R_c+r_b};\ R_2=\frac{R_{ekv}r_b}{R_{ekv}+R_c+r_b};\ R_{ekv.c}=\frac{(r_b+R_{ekv})R_c}{r_b+R_{ekv}+R_c}$

3. Modeling Program of Signals in Comparator Inputs

By applying the developed technique, the program of the signal modeling in ADC comparator circuits was developed. A simplified block diagram of the program is presented in Fig. 4. For the signal shape calculation in comparator inputs, it is accepted that parameters of all comparator impedances are equal and signal line losses are small. Signal shapes are considered in the dispersion-free frequency band.

When modeling transitional processes in the ADC analog circuits according to the presented block diagram of the program, the signal strip line geometry, wave parameters, layout of transistors and compatibility elements are optimized so that to reduce reflections up to the minimum and increase the converter accuracy and the operating speed.

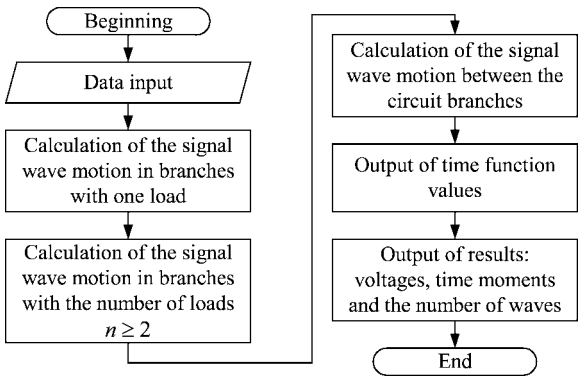

Fig. 4. A simplified block diagram of the signal modeling in ADC comparator circuits.

4. Results of Signal Modeling

Applying the developed calculation technique of the transitional process calculation for the microwave band ADC comparator circuit (Marcinkevičius, 2000) and the derived calculation algorithm (Marcinkevičius *et al.*, 2001), voltages in comparator inputs for two comparator circuits, when the comparator block number M_1 is equal to 8 and 16, were calculated. Diagrams of such circuits are presented in Figs. 5 and 6, respectively.

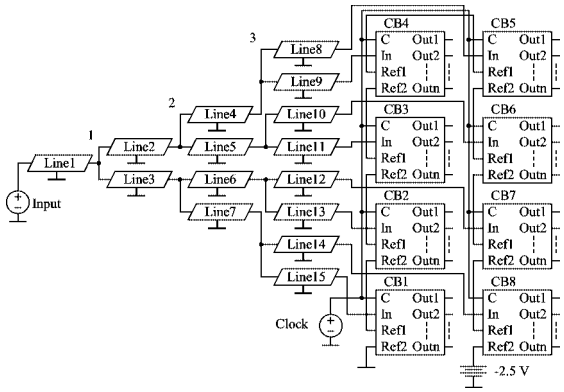

Fig. 5. Scheme of the comparator circuit when the number of comparator blocks is 8.

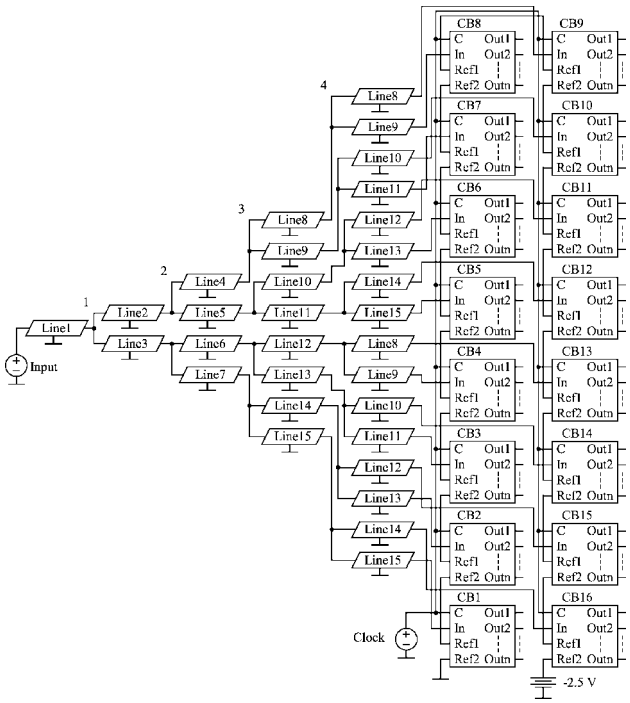

Fig. 6. Scheme of the comparator circuit when the number of comparator blocks is 16.

The signal circuit sections (Line 1, Line 2, etc), the ends of which are loaded with the comparator block inputs (CB1, CB2, . . ., CBn), are presented in the scheme. According to the circuit presented in Fig. 2, the 6-bit ADC comparator circuit, when comparators are connected into blocks in eights, is calculated. According to this circuit, the 8-bit ADC, when comparators are connected in sixteens, can also be calculated. According to the circuit presented in Fig. 3, the circuit of the 6-bit ADC comparator circuit, when comparators are connected into blocks in fours and in the case of 8-bit ADC when comparators are connected into blocks in eights, is calculated.

We will perform the voltage calculation for two cases when wave resistances of the circuit sections are equal ($Z_1 = Z_2 = Z_3 \ldots$) and in the quasi-compatibility mode when wave resistances are different ($Z_1 = 2Z_{2,3} = 4Z_{4\ldots7} = \ldots$). The 2.5 V amplitude signals whose front duration τ_f is equal to 1 ps and 10 ps are applied to inputs. The signal line maximum delay time $\tau_{\max}$ is 24 ps. Thus the ratio of the signal line maximum delay time to the signal front duration is $\tau_{\max}/\tau_f = 2.4$ and 0.24. The results of calculation of signal voltages of the ADC comparator circuit with 8 and 16 comparator blocks in the converter input and in inputs of comparator blocks are presented in Figs. 7 and 8, respectively.

The modeling results show that in the quasi-compatibility case the signal voltage fluctuation amplitude increases slightly ($\sim 1.5\%$) but fluctuations are damped during a shorter time ($\sim 40\%$ faster). Besides, it can be asserted that with the smaller num-

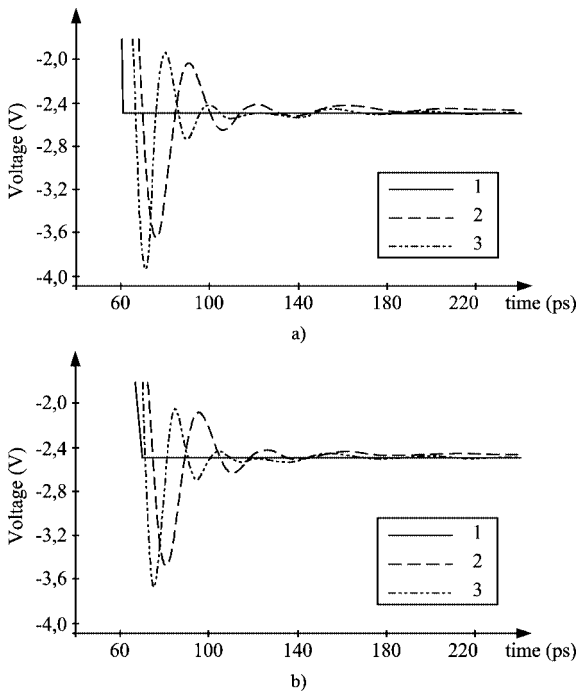

Fig. 7. Calculation results of the transitional process of the 6-bit ADC comparator circuit in which $M_1 = 8$ when: a) in inputs of comparator blocks when $\tau_{\max}/\tau_f = 2.4$; b) in inputs of comparator blocks when $\tau_{\max}/\tau_f = 0.24$ (here 1 – in the converter input; 2 – wave resistances of line sections are equal; 3 – in the quasi-compatibility case).

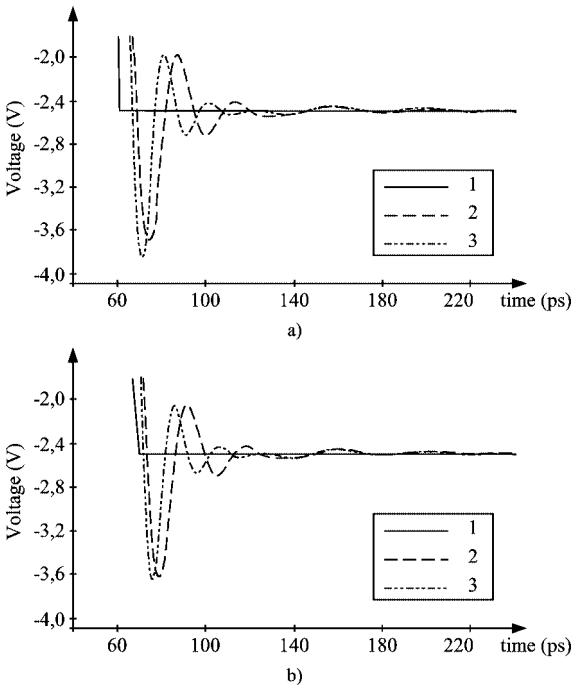

Fig. 8. Results of the voltage calculation of the 6-bit ADC comparator circuit in which $M_1 = 16$ when: a) in inputs of comparator blocks when $\tau_{\max}/\tau_f = 2.4$; b) in inputs of comparator blocks when $\tau_{\max}/\tau_f = 0.24$ (here 1 – in the converter input; 2 – wave resistances of line sections are equal; 3 – in the quasi-compatibility case).

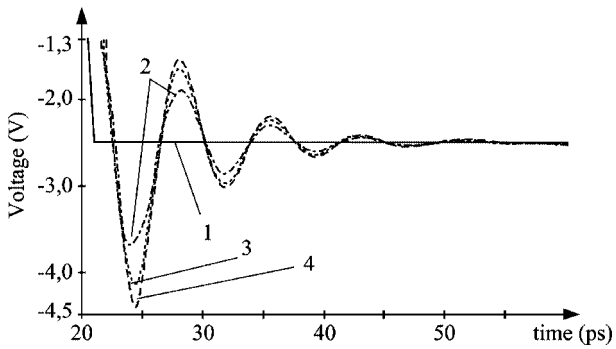

Fig. 9. Signal voltages in comparator inputs: 1 – the initial signal; 2 – at point "1"; 3 – at point "2"; 4 – at point "3" when $\tau_{\max}/\tau_f = 12$, $R_K = \infty$.

ber of comparators in a block the fluctuation amplitude and the damping time increase ($\sim 12\%$) because the total line length becomes longer and the number of branches, from which additional reflections are formed, increases. Therefore when designing the ADC comparator circuit, it is expedient to use quasi-compatible circuits, i.e., signal lines with different wave resistance.

The results obtained after the signal modeling in comparator circuits when loads of microstrip signal lines with distributed parameters – comparator complex impedances – are noncompatible with the wave resistance ($Z_{IN} = Z_0$) and when the load $R_K = Z_0$ is connected in series at the end of microstrip signal lines, i.e., in the quasi-compatibility mode, are presented in Figs. 9 and 10.

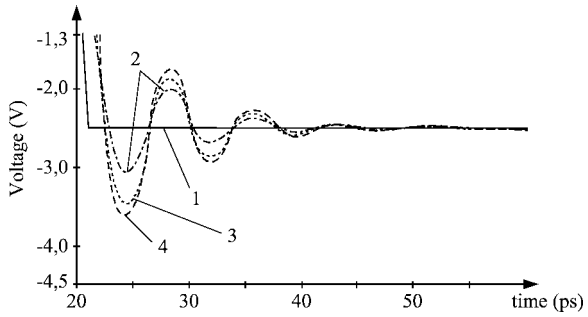

Fig. 10. Signal voltages in comparator inputs: 1 – the initial signal; 2 – at point "1"; 3 – at point "2"; 4 – at point "3" when $\tau_m ax/\tau_f = 12,\ R_K = Z_0$.

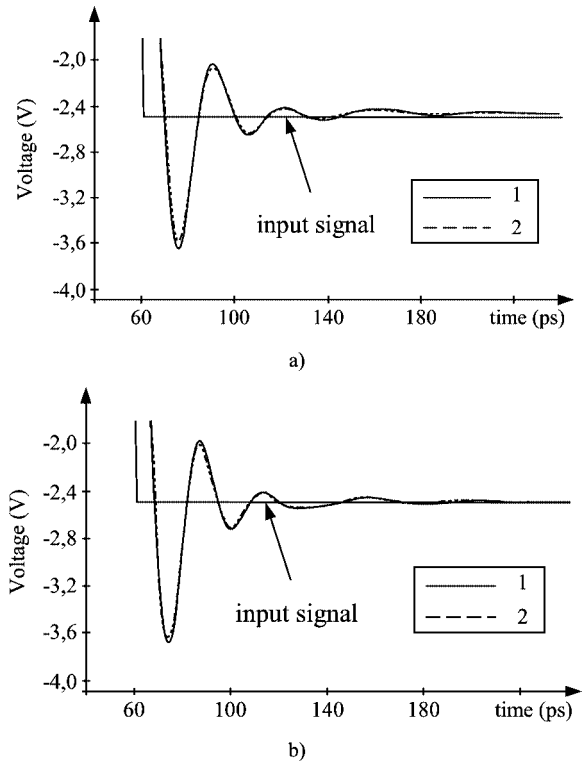

Fig. 11. Comparison of calculation results of the 6-bit ADC comparator circuit with 8 (a) and 16 (b) blocks: 1 – calculation using the PSpice program; 2 – calculation according to the derived algorithm.

The modeling results have shown that the connection of the additional load at the end of the line considerably reduces the signal form distortions: the transitional process time becomes shorter by $\sim 12\%$ and the transitional process amplitude decreases by $\sim 32\%$.

The calculation results obtained by applying the derived algorithm (Marcinkevičius *et al.*, 2001) were compared with the results attained using the PSpice program (Cadence, 2001). The calculations were performed on the computer of the following configuration: the AMD Athlon 1 GHz processor and the operating memory of 256 MB. Calculation results of the 6-bit ADC circuit, when the number of comparator blocks is 8 and 16, are presented in Fig. 11. The calculation time using the PSpice program was 31 and 55 hours, respectively. It is seen from the figure that the calculation results differ by 2% and the calculation time compared with that using the PSpice program became four times shorter. Thus we can assert that the ADC circuit calculation model is correct and the calculation algorithm is faster.

5. Conclusions

By applying the multiple reflection method, the generalized modeling algorithm of transition processes in ADC comparator circuits with distributed parameters has been created, the investigation of the signal dynamics depending on the layout parameters of the crystal components was carried out and layouts of wide-band circuits were proposed.

The mathematical model of the ADC comparator circuit has been created, with the help of which the computer calculation of the dynamics characteristics of the subnanosecond 6-bit ADC was performed.

Generalized algorithms of modeling the transfer functions of the ADC comparator circuit, according to which equations of these functions are composed in the automated way and signals in the comparator inputs are calculated, have been designed.

Peculiarities of transition processes in comparator inputs of the 6-bit ADC comparators have been investigated, and the effective influence of the impedance quasi-compatibility on the distortion reduction of subnanosecond voltage signals, when the front duration is lower than the delay time of the microstrip connection line, has been determined.

By using the developed technique, the calculation of transitional processes in the 6- and 8-bit gigahertz range ADC signal circuits has been performed. It has been determined that the transitional process quality in voltage inputs of comparator blocks strongly depends on the signal circuit layout architecture, the compatibility of line wave resistances and the number of branches up to comparator blocks.

The ADC speed can be increased by choosing the optimum number of comparator blocks in the circuit (e.g., in the 6-bit converter – 8 blocks with 8 comparators in each and in the 8-bit converter – 16 blocks with 16 comparators in each) using microstrip signal lines of different wave resistances.

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Signalų modeliavimas subnanosekundiniuose analoginiuose-skaitmeniniuose informacijos keitikliuose

Albinas MARCINKEVIČIUS, Darius POVILIAUSKAS

Sukurtas matematinis modelis ir metodika pereinamiesiems procesams apskaičiuoti integrinių ASK komparatorių signalinėse grandinėse taikant daugkartinių atspindžių metodą. Pateikti signalų modeliavimo rezultatai subnanosekundinių 6–8 skilčių ASK signalinėse grandinėse. Nustatyti komparatorių blokų įėjimuose pereinamojo proceso kokybės priklausomumai nuo signalinių mikrojuostelinių linijų banginių parametrų suderinamumo ir topologijos architektūros.

Taikant sukurtą metodiką atliktas 6 skilčių gigahercinio analoginio-skaitmeninio informacijos keitiklio topologijos optimizavimas ir perėjimo charakteristikų modeliavimas. Optimalus komparatorių ir signalo perdavimo mikrojuostelinių linijų išdėstymas luste ženkliai padidina keitiklio spartą. Pasiūlyta ASK komparatorių grandyno topologijos architektūra leidžia projektuoti 6–8 skilčių subnanosekundinius analoginius skaitmeninius informacijos keitiklius.