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A SIMULATION OF MICROPROCESSOR SYSTEMS FOR PARAMETER MEASUREMENTS OF THERMOPHYSICAL PROCESSES

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Abstract. The structure of a multimicroprocessor systems (MS) of M microprocessors (MP) and N blocks of random access memory (RAM) is presented. Probability techniques were applied to compile mathematical models which reflect random processes both in the whole structure and in its surroundings, as well as the links in the system units, specific operation features of the MP and the different data flows.

An analysis indicates that by simulations of MS in the preliminary and in the engineering stages of their design, when their behavior can be related to arbitrary parameters, universal evaluations of their operation can be achieved, lots of time, finance and human efforts can be saved.

Key words: microprocessor systems, computing structures, stochastic processes.

1. Introduction. One of important problems in disign of high capacity data-processing systems is the reduction of the queueing time of the MP seeking access to the RAM or to its specific blocks. The intended structures of MS must ensure limited-time solutions of a pre-given class, which is defined by the field of application. This can be achieved by making the system to fulfill a pre-defined number of orders per unit time that is by ensuring capacity for applied solutions on specified objects. Note that data flows in MS suffer of memory conflicts (Fung and Torng, 1979) when several MP apply simultaneously for acces to the RAM. An important feature of on-line microprocessor structures is the average time of the call of the i-th microprocessor queueing for the RAM. It is defined

as the delay between the access call and the exchange of data. Memory conflicts in such systems are mainly governed by the choice of the RAM. Memory conflicts can be minimized and avoided by applying high-speed RAM modes. On the other hand, semi-conductor storage units of high speed are very expensive. The additional spendings on hardware are excluded by using specific microprocessor – random – access memory links, as such systems need also high-speed control logic. This results in a wide application of limited speed RAM hardware, where for disign of large information sistems are applying mathematical models. Our survey of earlier publications indicates a shortage of efficient simulation techniques for the operation of microprocessor computing structures and their limited application in practical design.

Existing mathematical descriptions do not reflect the actual behaviour of data flows in calls of the MP for the RAM. Processes in the RAM blocks are not adequate to the operation structures. This is a challenge for the creation of extended mathematical models enabling a deeper analysis of microprocessor structures, as well as for the compilation of efficient engineering techniques for optimal designs of computing structures of this class.

2. The structure of a multimicroprocessor system with several random-access memory blocks. Microprocessors exchange data flows by one of several ways, including input-output channels, bus links and random-eccess memory blocks. Our survey suggests that application of the RAM is most popular because the approach gives several advantages. Note first of all the high capacity of MS, which come from the specific behaviour of the latter. We mean here the important difference of length between the memory cycle and the machine call cycle. In this approch several MP can operate on several memory imputs on the same level of MP copacity. The increased capacities of semiconductor storage blocks, the large operation speeds, the decreasing cost of informations storage – all theys speak for microprocessor structures with multi-block RAM. Let us consider MS which is shown in Fig. 1 with RAM of M blocks, with synchronization block (SB), with priorities block (PB), and M microprocessor blocks.

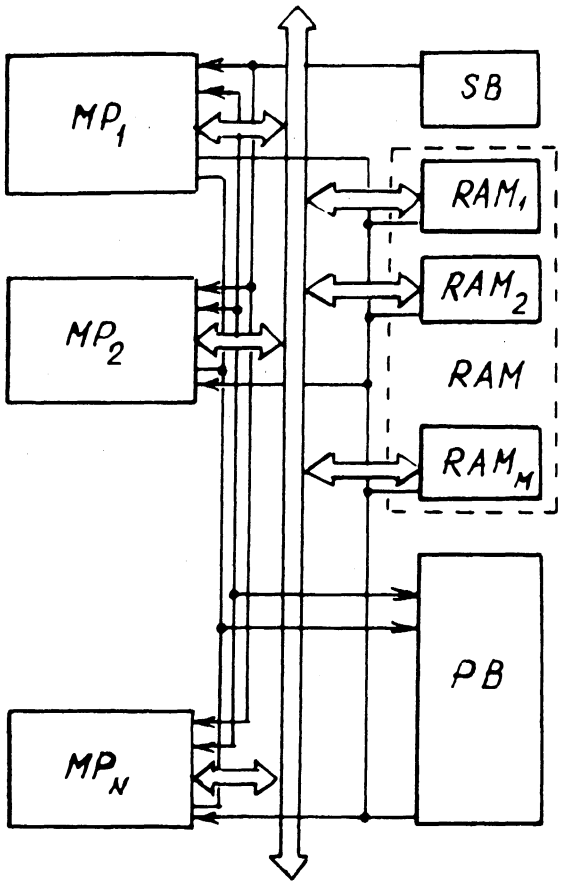

Fig. 1. The scheme of multiprocessor structure with M blocks of RAM.

All specific features of the structure, its internal communications and external influences evaluated, the microprocessor structure with a multi-block RAM can be described in terms of the theory of stochastic processes (Laurinavicius and Bielinskis, 1988) as closed-loop of service. It contains N data flows as calls for access and M service units (SU) with intermediate memories. The concept of such multimicroprocessor structure can be described as a cybernetic complex

$$G = \{X, S, Y, Z\}, \tag{1}$$

where $x_1, \ldots, x_v, \ldots, x_r \in X$ vector of external influences as descriptions of data processed, $s_1, \ldots, s_i, \ldots, s_k \in S$ sub-set of parameters important for the behaviour of the system, $y_1, \ldots, y_j, \ldots, y_l \in Y$ and $z_i, \ldots, z_u, \ldots, z_r \in Z$ – set of organization strategies for data processing and control, accordingly.

3. A behaviour simulation of a multimicroprocessor system. Let us consider a multimicroprocessor structure which is illustrated in Fig. 1 and include N microprocessors connected to M blocks of RAM. All MP have equal probabilities for calls an arbitrary blocks of the RAM. Memory conflicts are resolved on the no-priority approach. A block of the RAM serves only one of the queueing microprocessors at a time. The non-served MP repeat their calls. The repeated calls are issued at random intervals distributed exponentially with the intensity of the data flow λ. MP are served by each of the RAM blocks according to the law of Erlang $E_k(x)$. When the service time distribution function $G(x)$ is the Erlang distribution function of the k-th order

$$G(x) = E_k(x) = 1 - e^{-k\mu x} \sum_{j=0}^{k-1} \frac{(k\mu x)^j}{j!} \tag{2}$$

performance description of microprocessor structure can be described by general mathematical models and made adequate to actual processes in the system. To develop such a description, the phase approach must be applied and a phase space of the process must be selected. Let $\xi_i(t)$, $(i = \overline{1, M})$ be the number of phases which must pass all at the i-th block of the RAM queueing calls in time to before all they are served. With two RAM modes $\xi_i(t)$, $(i = 1, 2)$ and mark off

$$\xi(t) = \big(\xi_1(t), \xi_2(t)\big), \tag{3}$$

$$P_{(n_1,n_2)}(t) = P\{\xi(t) = (n_1, n_2)\} \tag{4}$$

performance of the system is described by equations.

$$\begin{aligned} & P_{(0,0)}(t+\Delta t) \\ =& P\{\xi(t+\Delta t)=(0,0)/\xi(t)=(0,0)\}P_{(0,0)}(t) \\ & + P\{\xi(t+\Delta t)=(0,0)/\xi(t)=(1,0)\}P_{(1,0)}(t) \\ & + P\{\xi(t+\Delta t)=(0,0)/\xi(t)=(0,1)\}P_{(0,1)}(t) \\ & + 0(\Delta t) = (1-N\lambda\Delta t)P_{(0,0)}(t) \\ & + (1-N\lambda\Delta t)k\mu\Delta t P_{(1,0)}(t) \\ & + (1-N\lambda\Delta t)k\mu\Delta t P_{(0,1)}(t) + 0(\Delta t). \end{aligned} \tag{5}$$

Now let us re-write the expression (5) become for $\Delta t \to 0$ and receive a differential equation

$$P'_{(0,0)}(t) = -N\lambda P_{(0,0)}(t) + k\mu P_{(1,0)}(t) + k\mu P_{(0,1)}(t). \tag{6}$$

Write $\rho = \lambda(k\mu)^{-1}$ and for $t \to \infty$ write the probability equation of the stable state

$$N_\rho P_{(0,0)} = P_{(1,0)} + P_{(0,1)}, \tag{7}$$

where

$$P_{(i,j)} = \lim_{t\to\infty} P_{(i,j)}(t) \quad (i,j=0,1). \tag{8}$$

For $1 \leqslant j_2 < k$ find

$$\begin{aligned} & P_{(0,j_2)}(t+\Delta t) \\ =& P\{\xi(t+\Delta t)=(0,j_2)/\xi(t)=(0,j_2)\}P_{(0,j_2)}(t) \\ & + P\{\xi(t+\Delta t)=(0,j_2)/\xi(t)=(0,j_2+1)\}P_{(0,j_2+1)}(t) \\ & + P\{\xi(t+\Delta t)=(0,j_2)/\xi(t)=(1,j_2)\}P_{(1,j_2)}(t) \\ & + 0(\Delta t) = \big[(1-(N-1)\lambda\Delta t\big](1-k\mu\Delta t)P_{(0,j_2)}(t) \\ & + \big[1-(N-1)\lambda\Delta t\big]k\mu\Delta t P_{(0,j_2+1)}(t) \\ & + \big[1-(N-1)\lambda\Delta t\big]k\mu\Delta t(1-k\mu\Delta t)P_{(1,j_2)}(t) \\ & + 0(\Delta t). \end{aligned} \tag{9}$$

Let us now re-write eguation (9)

$$P'_{(0,j_2)}(t) = -\big[(N-1)\lambda + k\mu\big]P_{(0,j_2)}(t) + k\mu P_{(0,j_2+1)}(t) + k\mu P_{(1,j_2)}(t). \tag{10}$$

Approach $t \to \infty$ and write

$$\lim_{t\to\infty} P_{(j_1,j_2)}(t) = P_{(j_1,j_2)}, \tag{11}$$

then define

$$\big[(N-1)\rho + 1\big]P_{(0,j_2)} = P_{(0,j_2+1)} + P_{(1,j_2)}. \tag{12}$$

In a similar manner, for $1 \leqslant j_1,\ j_2 < k$ find

$$\big[(N-1)\rho + 1\big]P_{(j_1,0)} = P_{j_1+1,0)} + P_{(j_1,1)}, \tag{13}$$

$$\big[(N-2)\rho + 2\big]P_{(j_1,j_2)} = P_{j_1+1,j_2)} + P_{(j_1,j_2+1)}, \tag{14}$$

For $0 \leqslant j_2 \leqslant k$ we obtain

$$\begin{aligned}
&P_{(k,j_2)}(t+\Delta t)\\
=&P\big\{\xi(t+\Delta t) = (k,j_2)/\xi(t) = (k,j_2)\big\}P_{(k,j_2)}(t)\\
&+P\big\{\xi(t+\Delta t) = (k,j_2)/\xi(t) = (k,j_2+1)\big\}P_{(k,j_2+1)}(t)\\
&+P\big\{\xi(t+\Delta t) = (k,j_2)/\xi(t) = (k+1,j_2)\big\}P_{(k+1,j_2)}(t)\\
&+P\big\{\xi(t+\Delta t) = (k,j_2)/\xi(t) = (0,j_2)\big\}P_{(0,j_2)}(t) + 0(\Delta t)\\
=&\big[1-(N-2)\lambda\Delta t\big](1-k\mu\Delta t)^2 P_{(k,j_2)}(t)\\
&+\big[1-(N-2)\lambda\Delta t\big](1-k\mu\Delta t)k\mu\Delta t P_{(k,j_2+1)}(t)\\
&+\big[1-(N-3)\lambda\Delta t\big](1-k\mu\Delta t)k\mu\Delta t P_{(k+1,j_2)}(t)\\
&+\frac{1}{2}(N-1)\lambda\Delta t(1-k\mu\Delta t)^2 P_{(0,j_2)}(t).
\end{aligned} \tag{15}$$

After some replacements eguation (15) becomes

$$\big[(N-2)\rho+2\big]P_{(k,j_2)} = P_{(k,j_2+1)} + P_{(k+1,j_2)} + \frac{1}{2}(N-1)\rho P_{0,j_2)}. \tag{16}$$

By an analogy for $0 \leqslant j_1 < k$

$$\big[(N-2)\rho+2\big]P_{(j_1,k)} = P_{(j_1+1,k)} + P_{(j_1,k+1)} + \frac{1}{2}(N-1)\rho P_{j_1,0)}, \tag{17}$$

and

$$\big[(N-2)\rho+2\big]P_{(k,k)} = P_{(k+1,k)} + P_{(k,k+1)} + \frac{1}{2}(N-1)\rho P_{0,k)} + \frac{1}{2}(N-1)\rho P_{(k,0)}. \tag{18}$$

In the general case for $n_1 = i_1 k + j_1$, $n_2 = i_2 k + j_2$, where $1 \leqslant i_1,\ i_2 \leqslant N-1$, $1 \leqslant j_1,\ j_2 \leqslant k$, $i_1 + i_2 \leqslant N-1$ find

$$\begin{aligned}
&P_{(n_1,n_2)}(t+\Delta t) = P_{(i_1k+j_1,i_2k+j_2)}(t+\Delta t)\\
&= P\big\{\xi(t+\Delta t) = (n_1,n_2)/\xi(t) = (n_1,n_2)\big\}P_{(n_1,n_2)}(t)\\
&\quad + P\big\{\xi(t+\Delta t)(n_1,n_2)/\xi(t) = (n_1+1,n_2)\big\}P_{(n_1+1,n_2)}(t)\\
&\quad + P\{\xi(t+\Delta t)(n_1,n_2)/\xi(t) = (n_1,n_2+1)\big\}P_{(n_1,n_2+1)}(t)\\
&\quad + P\big\{\xi(t+\Delta t)(n_1,n_2)/\xi(t) = (n_1-k,n_2)\big\}P_{(n_1-k,n_2)}(t)\\
&\quad + P\big\{\xi(t+\Delta t)(n_1,n_2)/\xi(t) = (n_1,n_2-k)\big\}P_{(n_1,n_2-k)}(t)\\
&\quad + 0(\Delta t)\\
&= \big[1-(N-i_1-i_2-2)\lambda\Delta t\big](1-k\mu\Delta t)^2 P_{(n_1,n_2)}(t)\\
&\quad + \big[1-(N-i_1-i_2-2)\lambda\Delta t\big](1-k\mu\Delta t)k\mu\Delta t P_{(n_1+1,n_2)}(t)\\
&\quad + \big[1-(N-i_1-i_2-2)\lambda\Delta t\big](1-k\mu\Delta t)k\mu\Delta t P_{(n_1,n_2+1)}(t)\\
&\quad + \frac{1}{2}(N-i_1-i_2-1)\lambda\Delta t(1-k\mu\Delta t)^2 P_{(n_1-k,n_2)}(t)\\
&\quad + \frac{1}{2}(N-i_1-i_2-1)\lambda\Delta t(1-k\mu\Delta t)^2 P_{(n_1,n_2-k)}(t)\\
&\quad + 0(\Delta t).
\end{aligned} \tag{19}$$

Here $P_{(n_1+1,n_2)}(t) = P_{(n_1,n_2+1)}(t) = 0$, if $n_1 + n_2 = Nk$.
After some replacements find

$$\begin{aligned}\left[((N-2-i_1-i_2)\rho+2\right]P_{(i_1,k+j_1,i_2k+j_2)} &= P_{(i_1k+j_1+1,i_2k+j_2)} + P_{(i_1k+j_1,i_2k+j_2+1)} \\ &+ \frac{1}{2}(N-1-i_1-i_2)\rho P_{((i_1-1)k+j_1,i_2k+j_2)} \\ &+ \frac{1}{2}(N-i_1-i_2-1)\rho P_{(i,k+j_1,(i_2-1)k+j_2)}, \end{aligned} \tag{20}$$

for $1 \leqslant i_1,\ i_2 \leqslant N-1;\ 1 \leqslant j_1,\ j_2 \leqslant k;\ i_1 + i_2 \leqslant N-1$.
From received relations together with condition

$$\sum_{(n_1,n_2)} P_{(n_1,n_2)} = 1, \tag{21}$$

in accordance with created algorithm and program were find probabilities $P_{(n_1,n_2)}$ of RAM having n calls of microprocessors

$$Q_n = \sum_{n_1+n_2=n} P_{(n_1,n_2)}, \tag{22}$$

which often are described by Q_k $(k = \overline{1,N})$, the average number of microprocessors R_v queueing for the RAM, probability of no microprocessors calls $_0$ waiting at the RAM. The suggested relations, if reasonably applied, can give the probabilities of arbitrary states of the system, that is, any parameter of the microprocessor structure. Now we introduce the $\rho = -\frac{\lambda}{\mu}$ term and assume real values $\lambda = 1.10^6$ op/sec, and $\mu = 0.2 \cdot 10^7$ op/sec, and find relations of microprocessor structures characteristics from various parameters. Fig. 2 presents relations of curves for probability $Q_0 = f(N,\rho)$ of no calls to RAM from N for $\rho(1-\rho = 0.1;\ 2-\rho = 0.2;\ 3-\rho = 0.3;\ 4-\rho = 0.5;\ 5-\rho = 0.6;\ 6-\rho = 0.9)$ Fig. 3 shows relations of curves for probability $Q_0 = f(\rho,N)$ of no calls to RAM from ρ for $N(1-N = 1;\ 2-N = 3;\ 3-N = 6;\ 4-N = 9;\ 5-N = 12;\ 6-N = 15)$. Fig. 4 gives

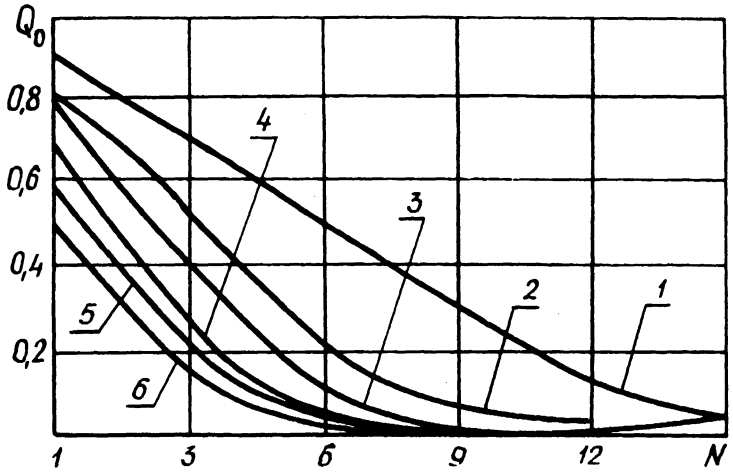

Fig. 2. Curves for probabiliy $Q_0 = f(N, \rho)$ of no calls to RAM from N for various ρ.

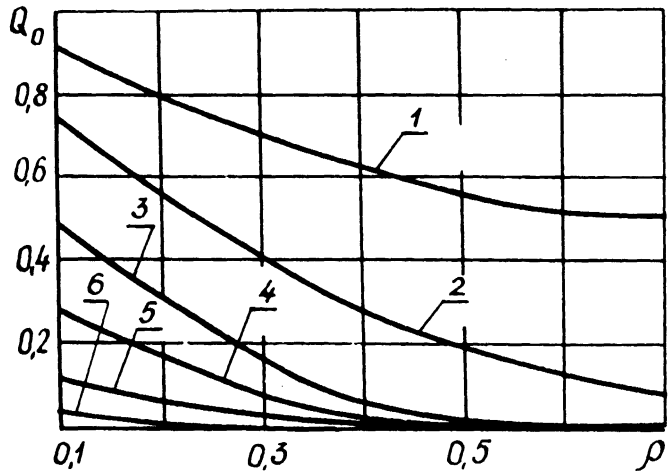

Fig. 3. Curves for probabiliy $Q_0 = f(\rho, N)$ of no calls to RAM from ρ for various N.

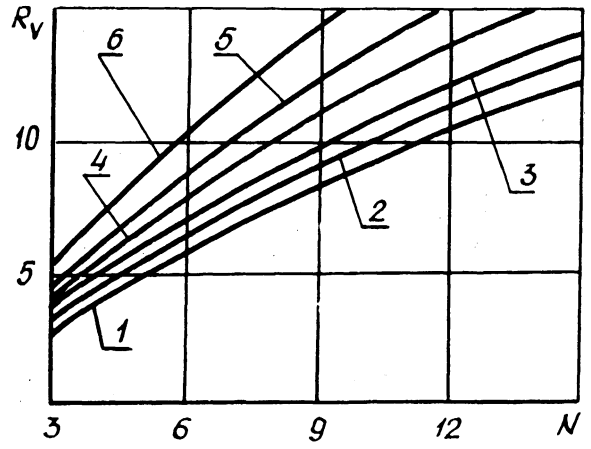

Fig. 4. Curves of the average number of queueing microprocessors $R_v = f(N, \rho)$ from N for various ρ.

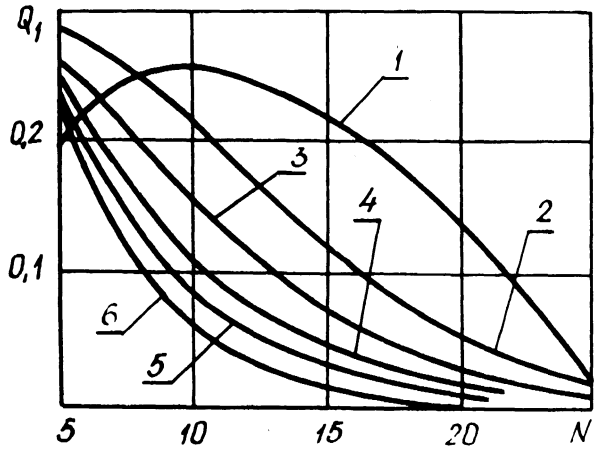

Fig. 5. Curves for the $Q_1^{(2)} = f(N, \rho)$ probabiliy of $k = 1$ queueing microprocessors at a two-blocks RAM from N for various ρ.

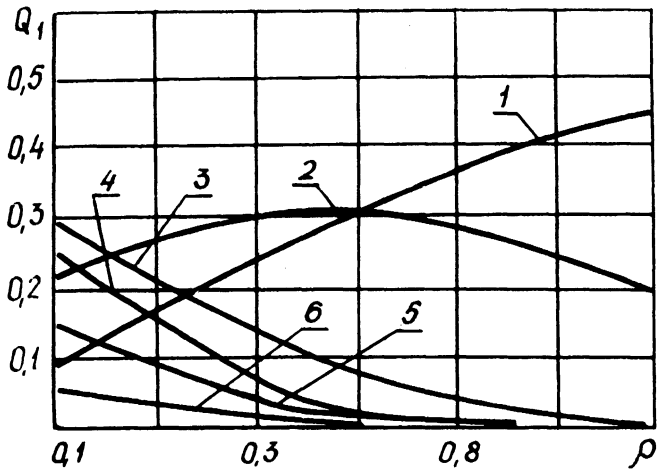

Fig. 6. Curves of the $Q_1 = f(\rho, N)$ probability of $k = 1$ calls to RAM from ρ for various N.

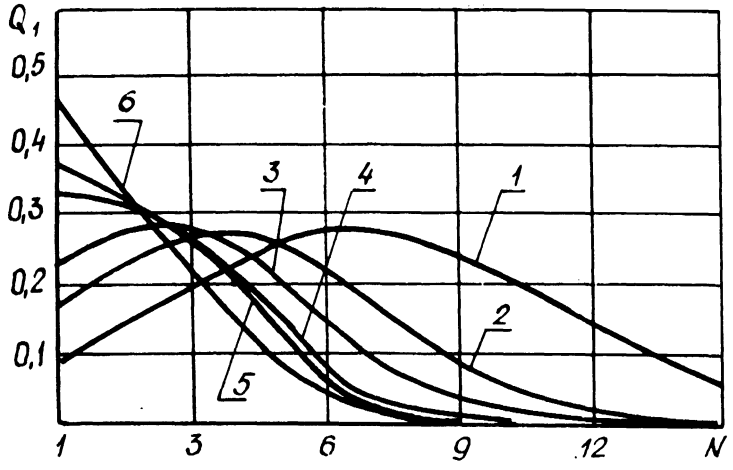

Fig. 7. Curves for the $Q_1^{(2)} = f(N, \rho)$ probabiliy of $k = 1$ queueing microprocessors from N for various ρ.

relations of curves of the average number of queueing, microprocessors $R_v = f(N, \rho)$ from N for $\rho(1 - \rho = 0.1;\ 2 - \rho = 0.2;\ 3 - \rho = 0.3;\ 4 - \rho = 0.5;\ 5 - \rho = 0.6;\ 6 - \rho = 0.9)$. Fig. 5 presents relations of curves for the $Q_1^{(2)} = f(N, \rho)$ probability of $k = 1$ queueing microprocessors at a two-block RAM from N for $\rho(1 - \rho = 0.1;\ 2 - \rho = 0.2;\ 3 - \rho = 0.3;\ 4 - \rho = 0.5;\ 5 - \rho = 0.6;\ 6 - \rho = 0.9)$. Fig. 6 gives dependency of curves for the $Q_1 = f(\rho, N)$ probability of $k = 1$ queueing microprocessors from for $N(1 - N = 1;\ 2 - N = 3;\ 3 - N = 6;\ 4 - N = 9;\ 5 - N = 12;\ 6 - N = 15)$. Fig. 7 shows relations of curves for the $Q_1 = f(N, \rho)$ probability of $k = 1$ gueueing microprocessors from N for $\rho(1 - \rho = 0.1;\ 2 - \rho = 0.2;\ 3 - \rho = 0.3;\ 4 - \rho = 0.5;\ 5 - \rho = 0.6;\ 6 - \rho = 0.9)$.

4. Conclusions. Analytical expressions suggested for the behaviour of microprocessor structures related to a number of performance parameters and of external influences permit to ascertain the eficiency of the system which depend on the number of MP and their operation speed, features of the data flow, to the number RAM blocks and their operation speed.

Mathematical models of MP are suggested and they reflect data axchange between RAM and the microprocessors. The suggested technique of parameter evaluation enables the choice of reasonable structures in the early stages of their desing, of the components of microprocessors to be included, of the number of the RAM blocks for the pre-chosen efficiency of the system. The analysis locates the largest loads and evaluates their influence on the performance of the system, and facilitates the choice of performance parameters, of the structure and of the most reasonable operation mode in the preliminary stage and during the engineering design. As suggested by the simulation, a significantly increased number of the MP causes a serious increase of the queueing time as well as memory conflicts in the overloaded RAM memory. This is an important disadvantage to the efficiency of microprocessor structures. To increase information permitability in such systems, the number of calls sources and the probability of access to the RAM must be reasonably reduced either by storing a certain part of software and data in the local memory

of the MP, or by increasing the amount and the performance speed of the RAM. The results of both the mathematical simulation and the qualitative relations of multimicroprocessor structures to their different parameters are intended for optimal design of microprocessor systems.

REFERENCES

Fung, K.T., and H.C.Torng (1979). On the analysis of memory complicts and bus contentions in multimicroprocessors systems. *JEEE trans. on computers*, **27**(1), 28–37.

Laurinavičius, A., and F.Bielinskis (1988). Simulation of microprocessors structures for investigation of heat processes. *Works of the Academy of Sciences the Lithuanian SSR*, Ser.B **3**(166), 29–34 (in Russian).

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